FIG. 1

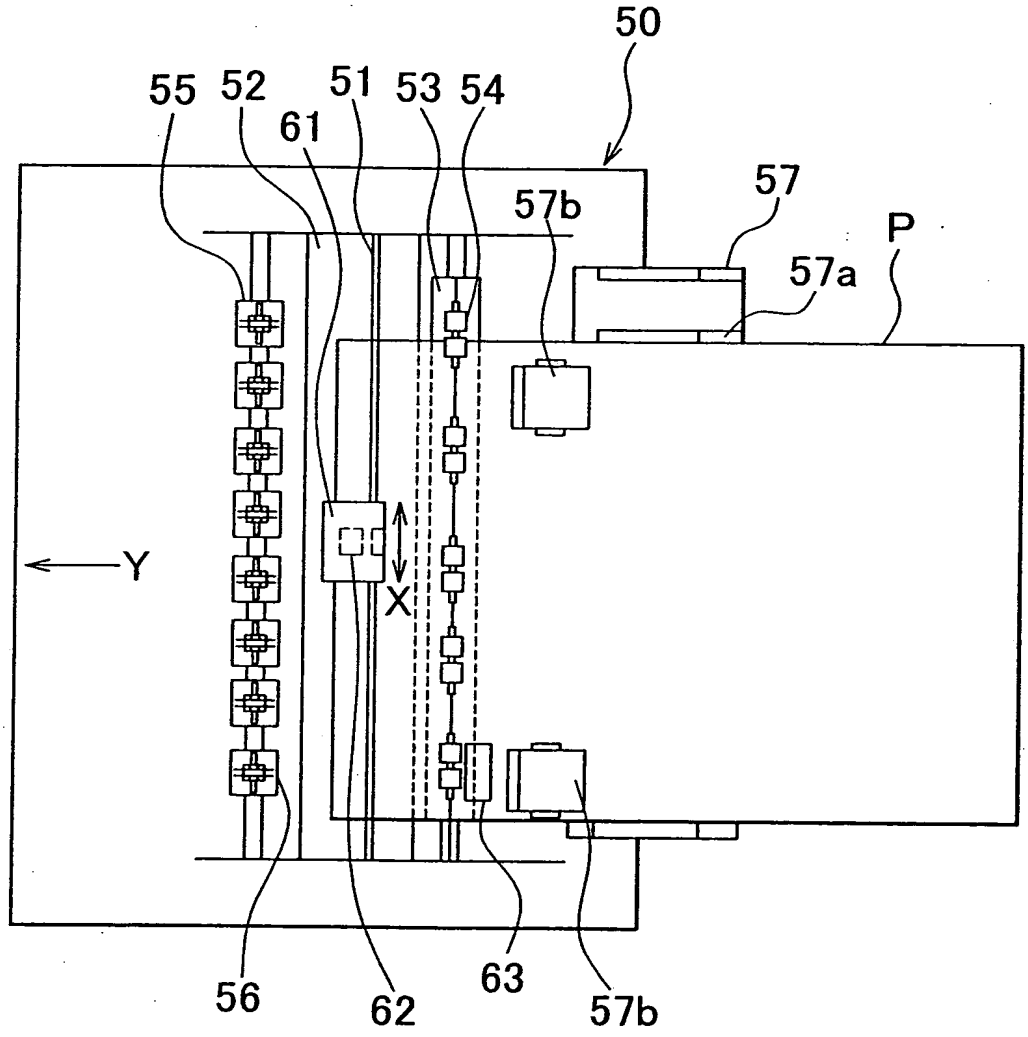


FIG. 2

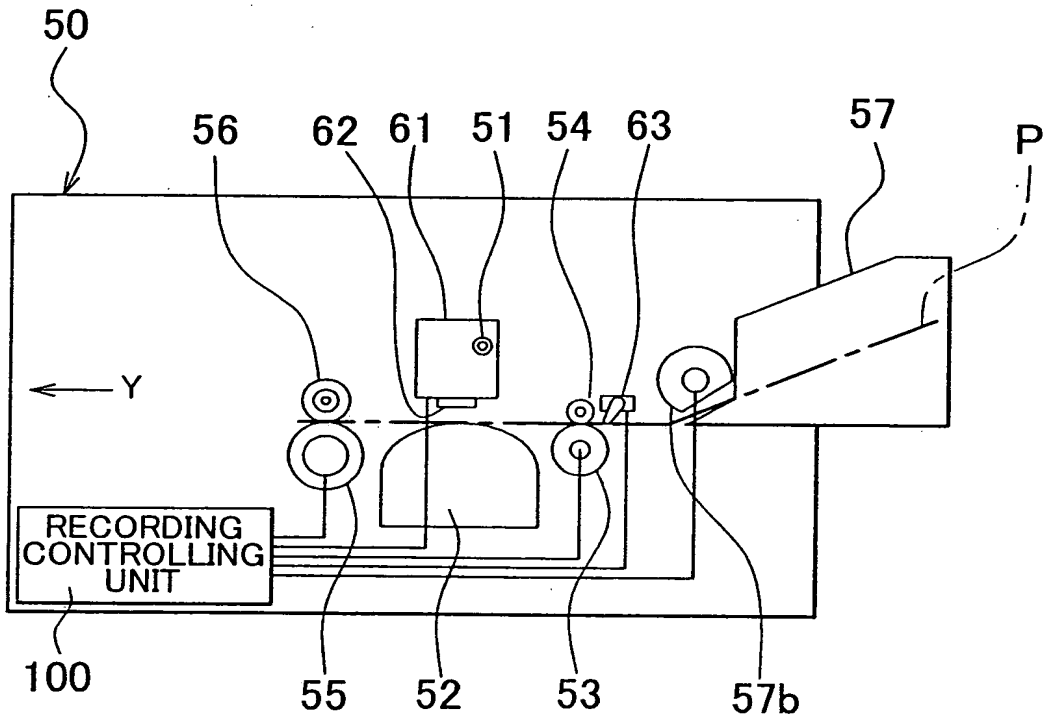

50
56
62
61
51
54
63
57
P
Y
RECORDING CONTROLLING UNIT
100
55
52
53
57b

FIG. 3

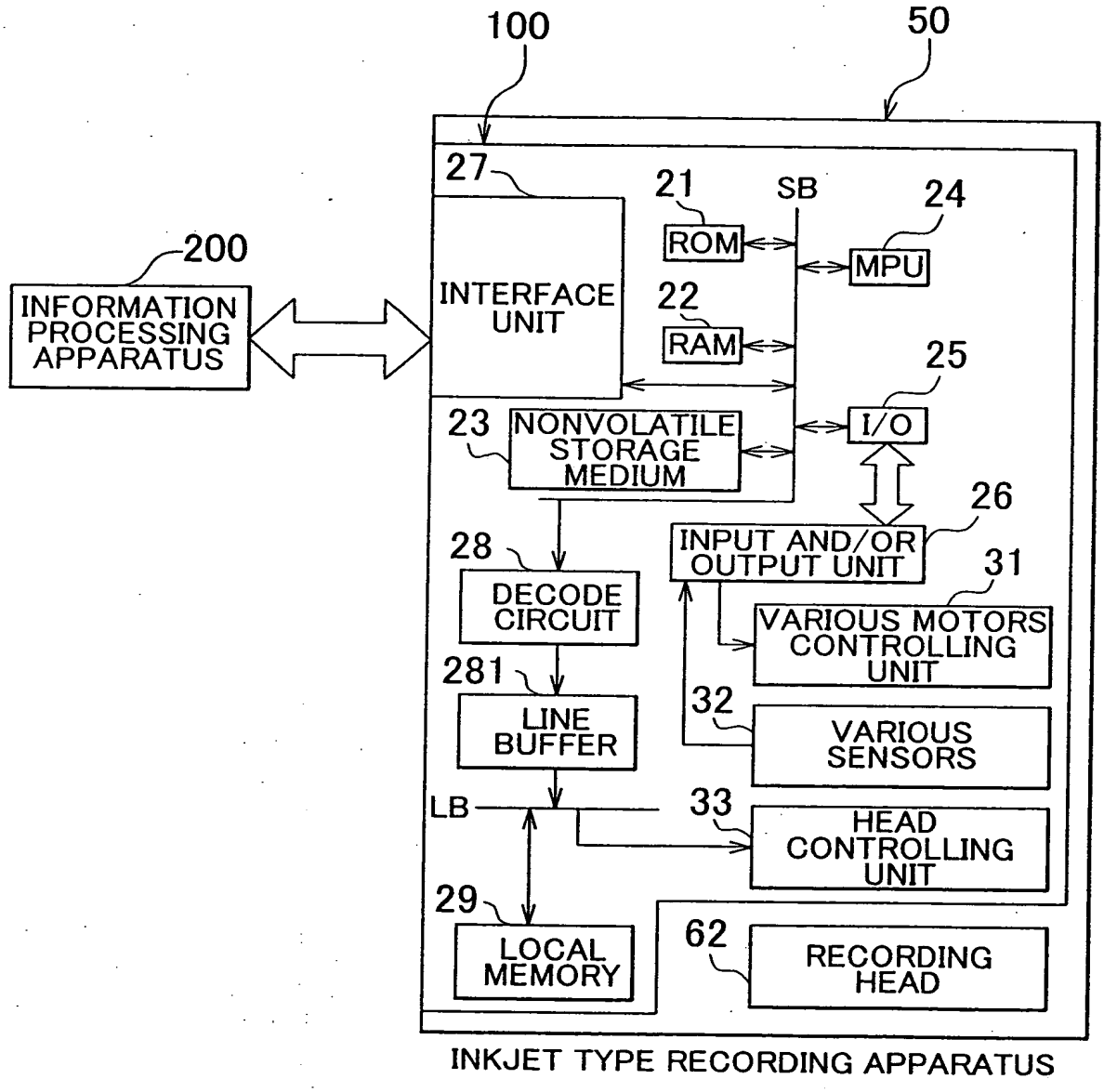

100
50
27
21
SB
24
200
ROM
MPU
INFORMATION PROCESSING APPARATUS
INTERFACE UNIT
22
RAM
25
23
NONVOLATILE STORAGE MEDIUM
I/O
26
INPUT AND/OR OUTPUT UNIT
28
31
DECODE CIRCUIT
VARIOUS MOTORS CONTROLLING UNIT
281
32
LINE BUFFER
VARIOUS SENSORS
LB
33
HEAD CONTROLLING UNIT
29
62
LOCAL MEMORY
RECORDING HEAD
INKJET TYPE RECORDING APPARATUS

FIG. 4

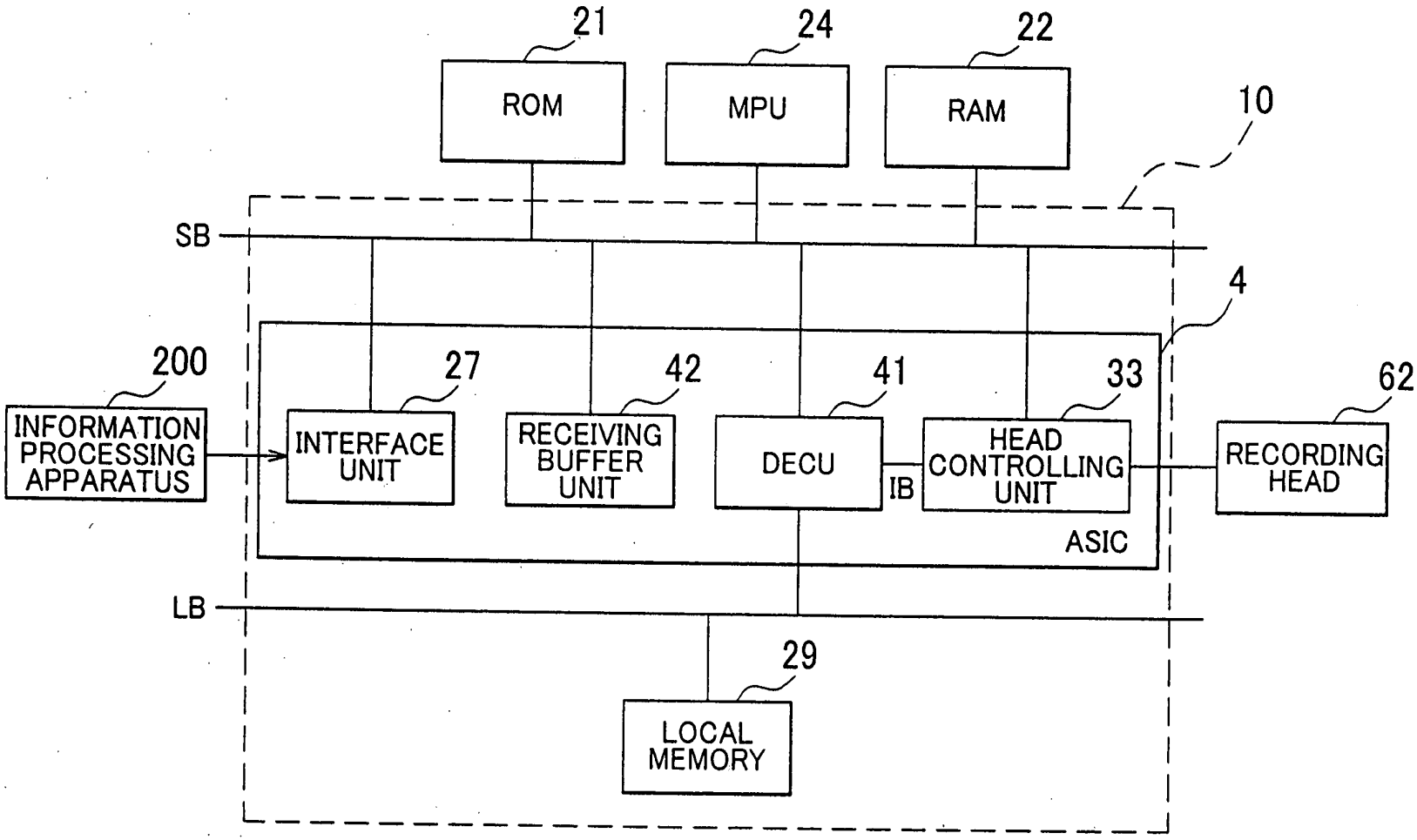

21
24
22
ROM
MPU
RAM
10
SB
4
200
27
42
41
33
62
INFORMATION PROCESSING APPARATUS
INTERFACE UNIT
RECEIVING BUFFER UNIT
DECU
IB
HEAD CONTROLLING UNIT
RECORDING HEAD
ASIC
LB
29
LOCAL MEMORY

FIG. 5

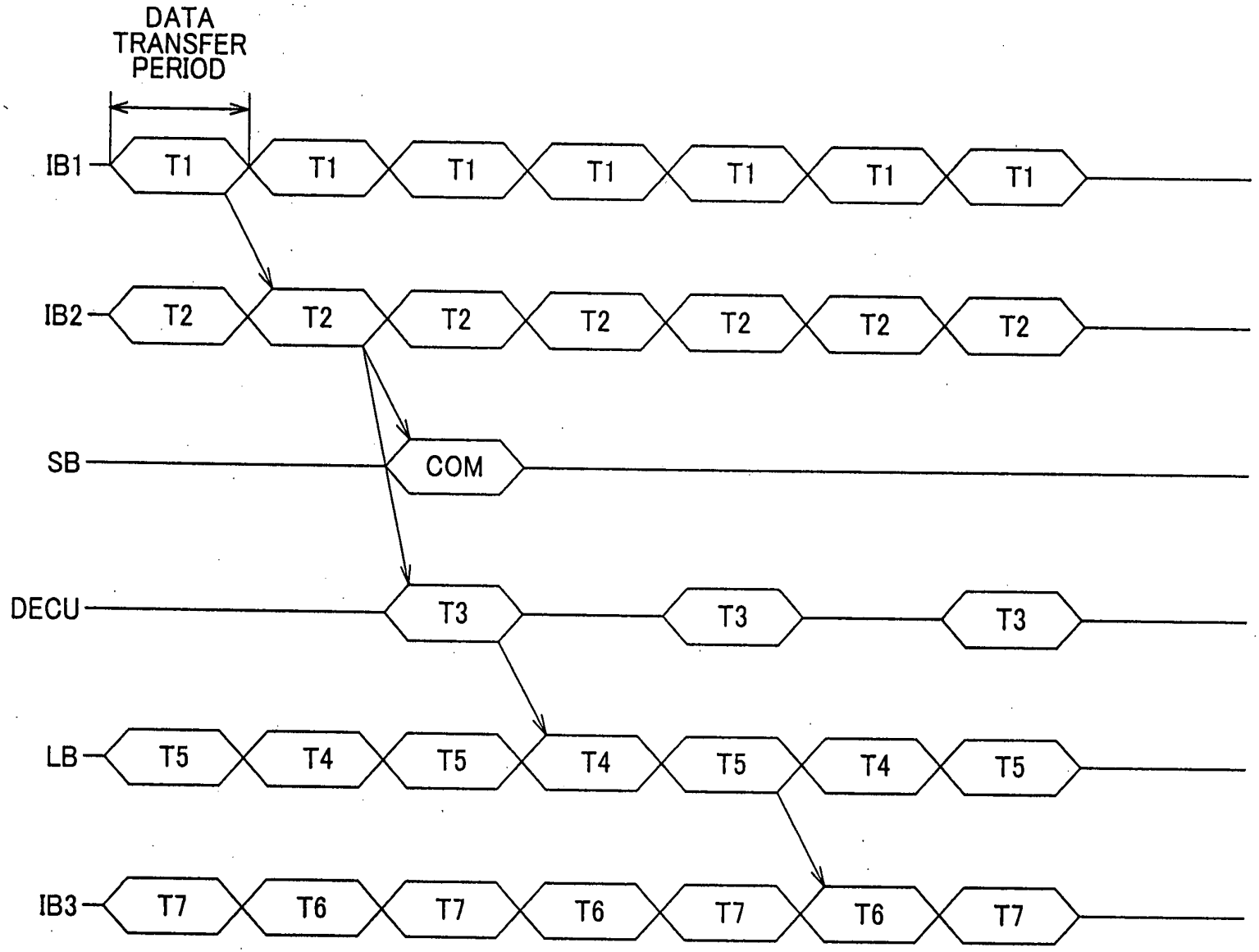

DATA
TRANSFER
PERIOD
IB1
T1
T1
T1
T1
T1
T1
T1
IB2
T2
T2
T2
T2
T2
T2
T2
SB
COM
DECU
T3
T3
T3
LB
T5
T4
T5
T4
T5
T4
T5
IB3
T7
T6
T7
T6
T7
T6
T7

FIG. 6

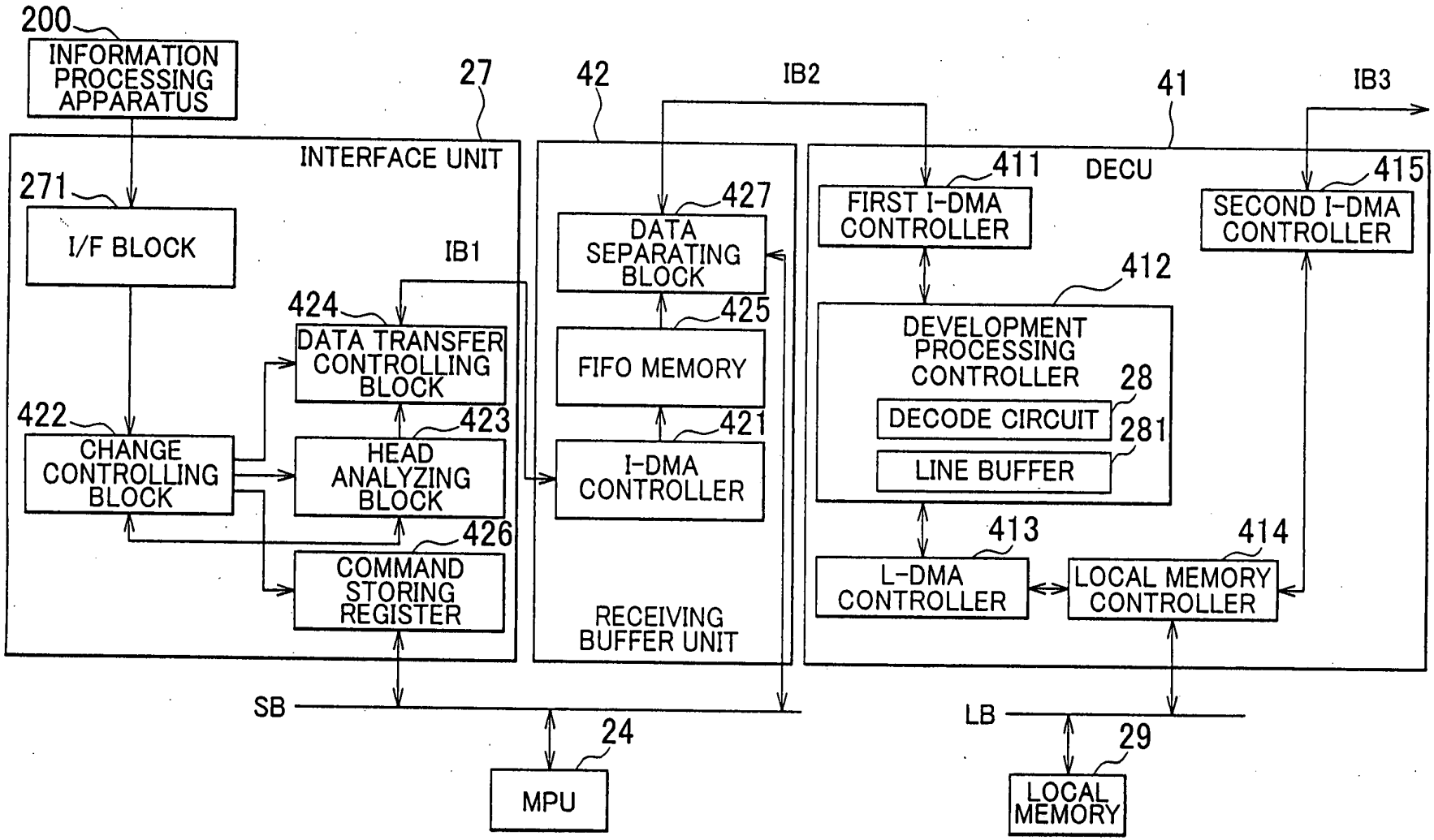

200
INFORMATION PROCESSING APPARATUS
27
INTERFACE UNIT
271
I/F BLOCK
IB1
424
DATA TRANSFER CONTROLLING BLOCK
422
CHANGE CONTROLLING BLOCK
423
HEAD ANALYZING BLOCK
426
COMMAND STORING REGISTER
42
IB2
427
DATA SEPARATING BLOCK
425
FIFO MEMORY
421
I-DMA CONTROLLER
RECEIVING BUFFER UNIT
41
IB3
DECU
411
FIRST I-DMA CONTROLLER
415
SECOND I-DMA CONTROLLER
412
DEVELOPMENT PROCESSING CONTROLLER
28
DECODE CIRCUIT
281
LINE BUFFER
413
L-DMA CONTROLLER
414
LOCAL MEMORY CONTROLLER
SB
24
MPU
LB
29
LOCAL MEMORY

FIG. 7

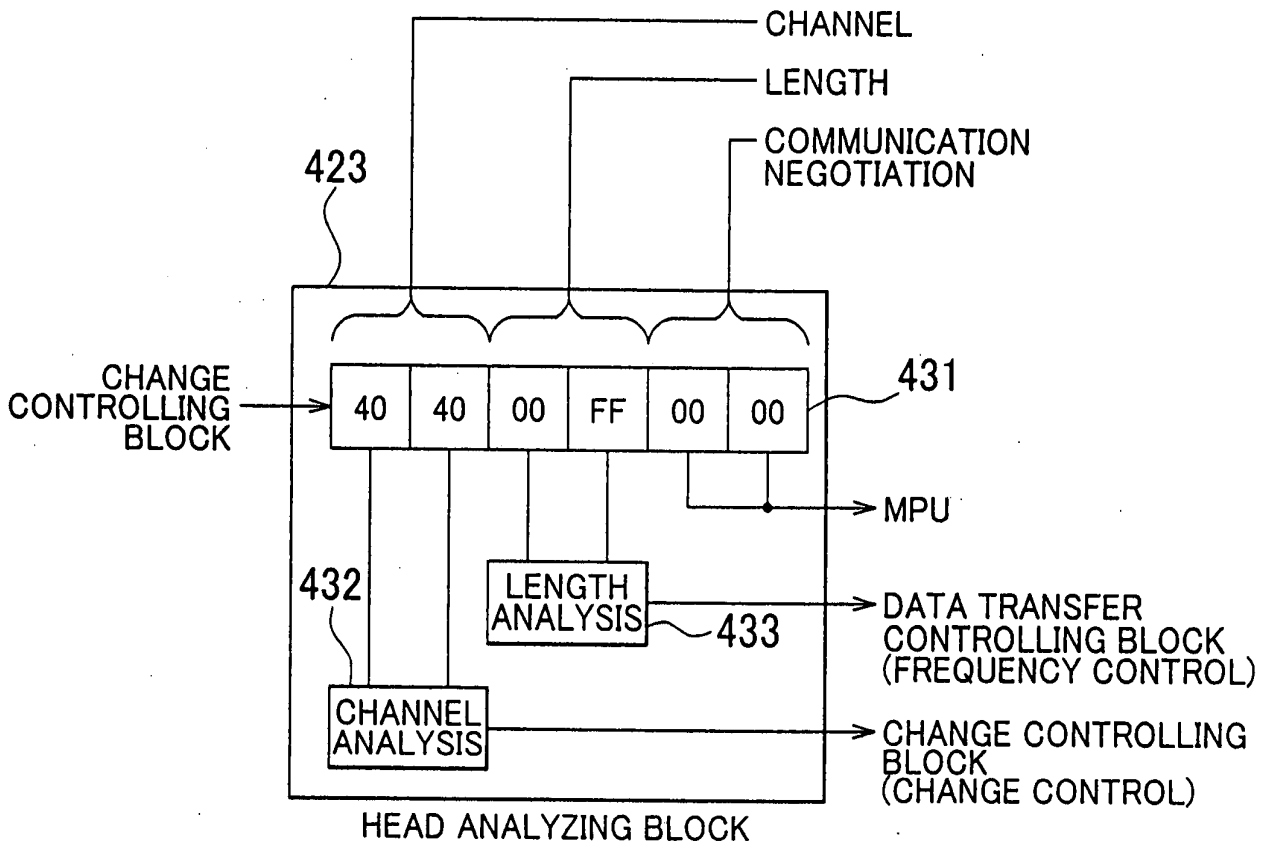

CHANNEL
LENGTH
COMMUNICATION NEGOTIATION
423
CHANGE CONTROLLING BLOCK
40
40
00
FF
00
00
431
MPU
432
LENGTH ANALYSIS
433
DATA TRANSFER CONTROLLING BLOCK (FREQUENCY CONTROL)
CHANNEL ANALYSIS
CHANGE CONTROLLING BLOCK (CHANGE CONTROL)
HEAD ANALYZING BLOCK

FIG. 8

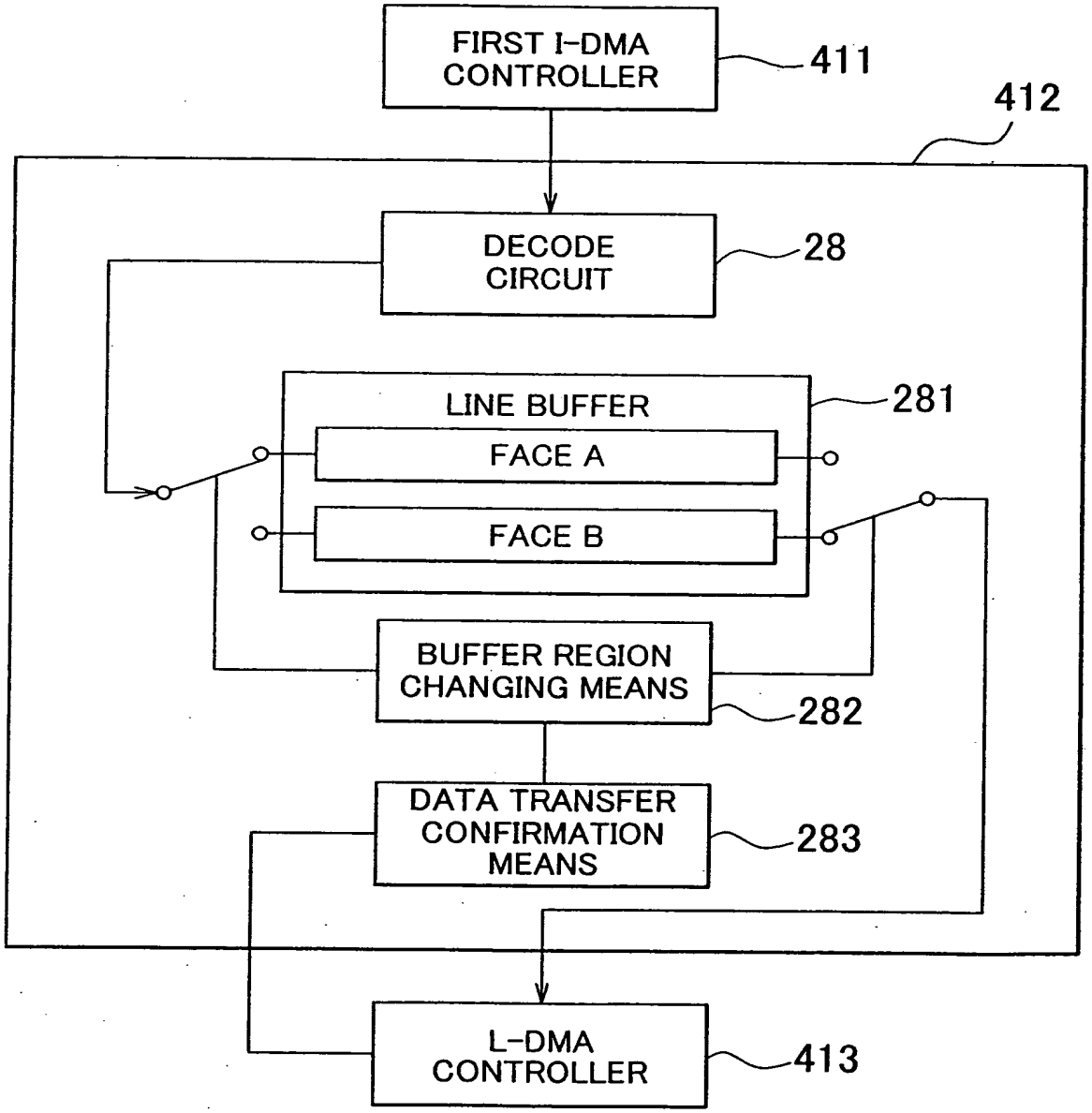
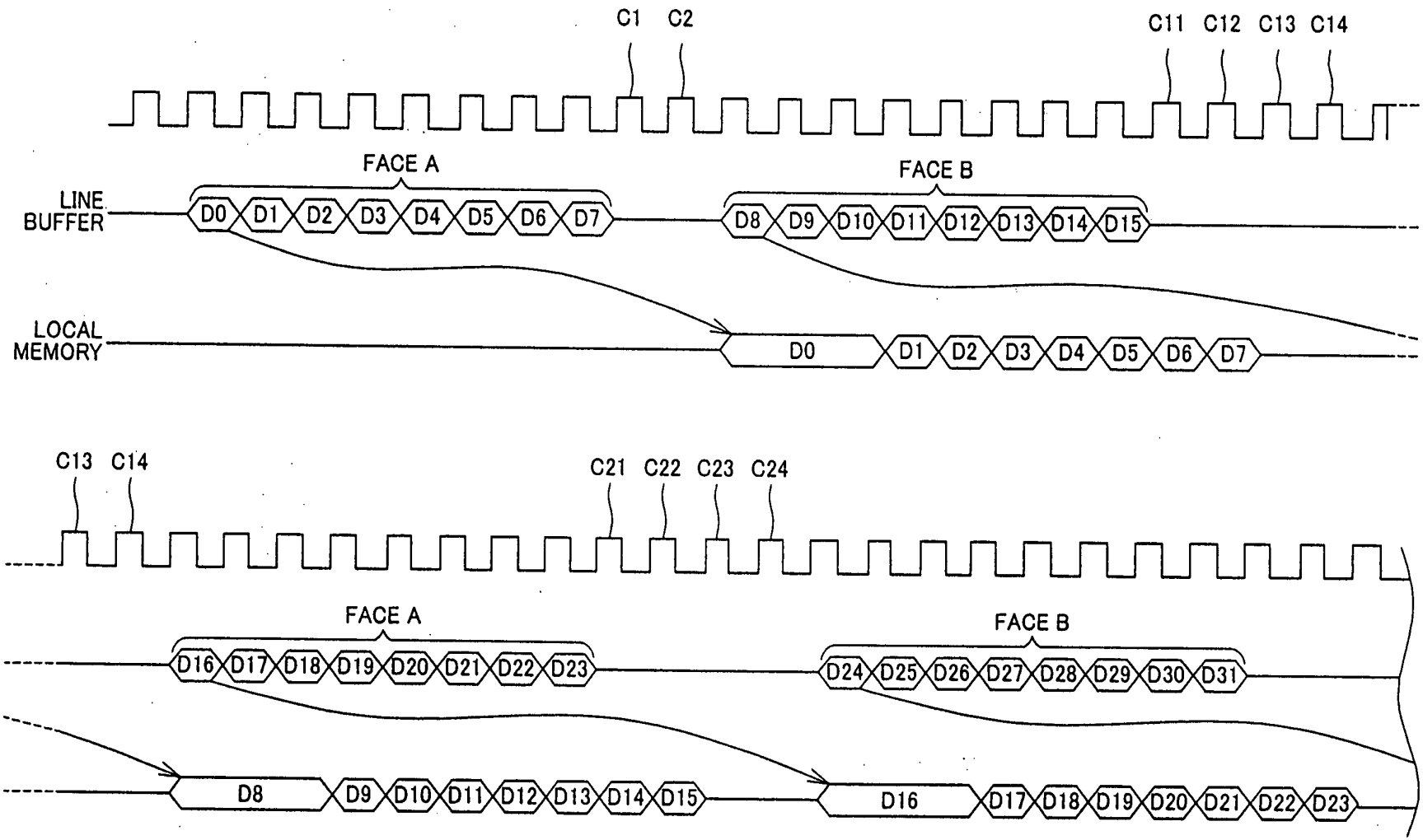

FIRST I-DMA CONTROLLER
411
412
DECODE CIRCUIT
28
LINE BUFFER
281
FACE A
FACE B
BUFFER REGION CHANGING MEANS
282
DATA TRANSFER CONFIRMATION MEANS
283
L-DMA CONTROLLER
413

FIG. 9


C1
C2
C11
C12
C13
C14
FACE A
FACE B
LINE BUFFER
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
LOCAL MEMORY
C13
C14
C21
C22
C23
C24
FACE A
FACE B
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23

F I G. 10

OPERATION CONDITION
MAIN MEMORY SIDE : STARTING ADDRESS OF RUN LENGTH DATA IS AN EVEN ADDRESS
LOCAL MEMORY SIDE : STARTING ADDRESS OF IMAGE DATA IS AN EVEN ADDRESS
NUMBER OF BYTES IN 1 LINE : 16 BYTES

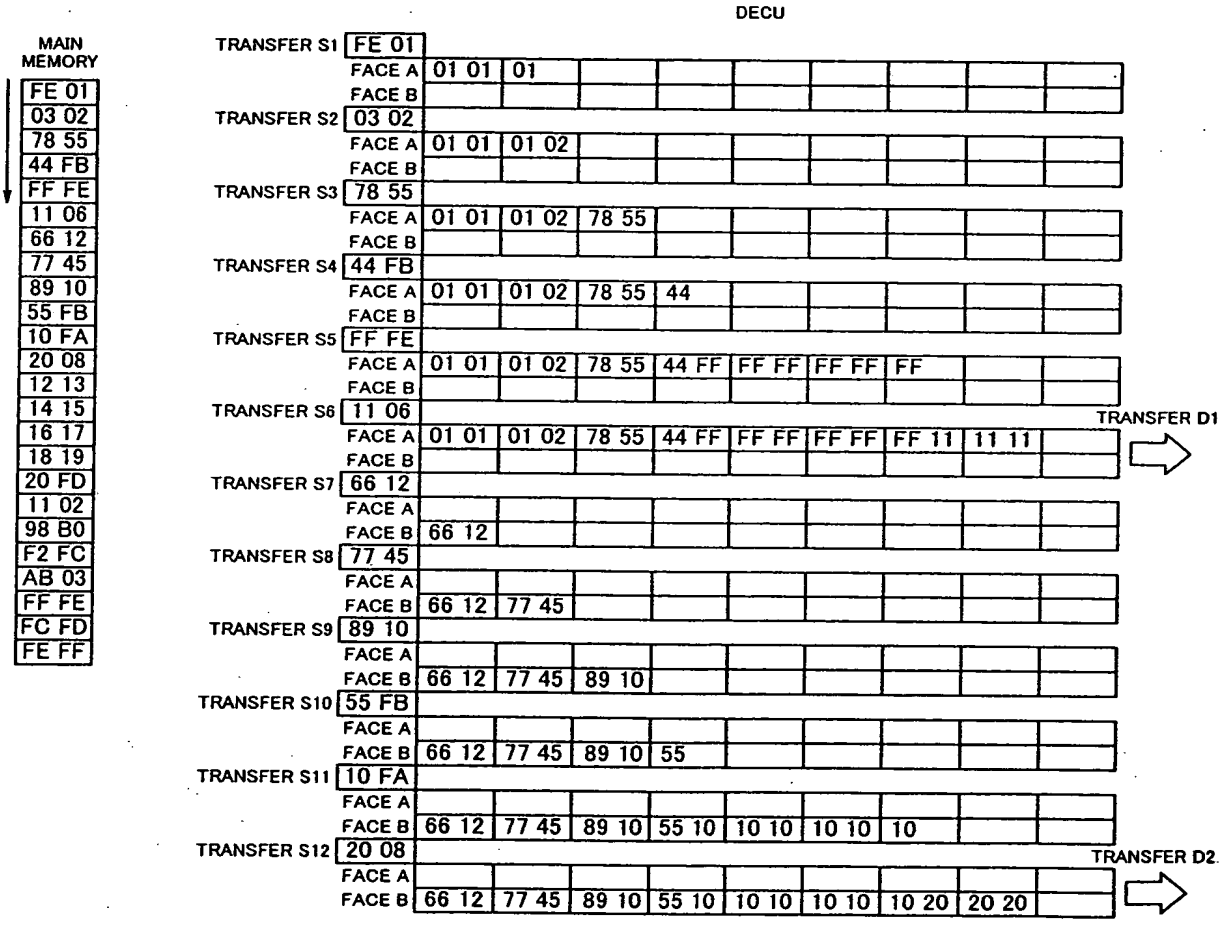
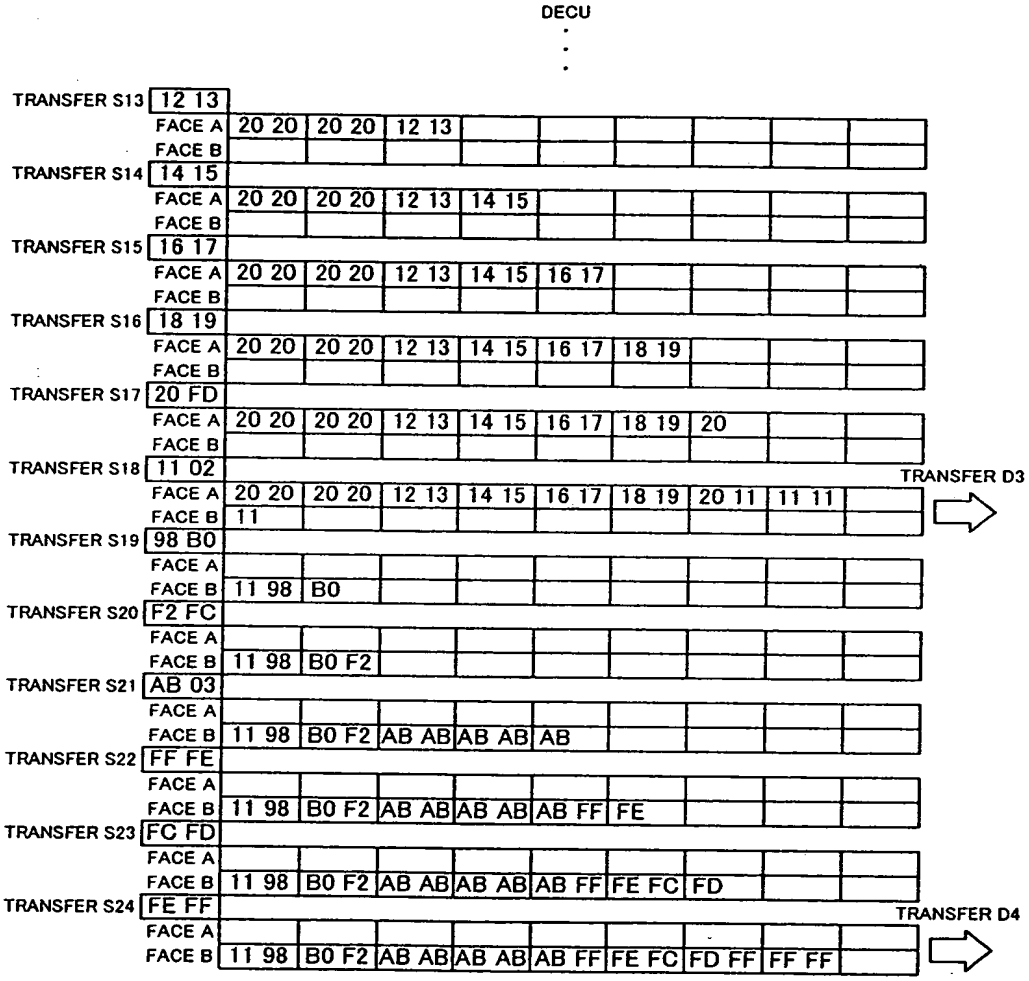


FIG. 11


DECU
TRANSFER S13
12 13
FACE A
20 20
20 20
12 13
FACE B
TRANSFER S14
14 15
FACE A
20 20
20 20
12 13
14 15
FACE B
TRANSFER S15
16 17
FACE A
20 20
20 20
12 13
14 15
16 17
FACE B
TRANSFER S16
18 19
FACE A
20 20
20 20
12 13
14 15
16 17
18 19
FACE B
TRANSFER S17
20 FD
FACE A
20 20
20 20
12 13
14 15
16 17
18 19
20
FACE B
TRANSFER S18
11 02
TRANSFER D3
FACE A
20 20
20 20
12 13
14 15
16 17
18 19
20 11
11 11
FACE B
11
TRANSFER S19
98 B0
FACE A
FACE B
11 98
B0
TRANSFER S20
F2 FC
FACE A
FACE B
11 98
B0 F2
TRANSFER S21
AB 03
FACE A
FACE B
11 98
B0 F2
AB AB
AB AB
AB
TRANSFER S22
FF FE
FACE A
FACE B
11 98
B0 F2
AB AB
AB AB
AB FF
FE
TRANSFER S23
FC FD
FACE A
FACE B
11 98
B0 F2
AB AB
AB AB
AB FF
FE FC
FD
TRANSFER S24
FE FF
TRANSFER D4
FACE A
FACE B
11 98
B0 F2
AB AB
AB AB
AB FF
FE FC
FD FF
FF FF

SETTING CONDITION
NO VERTICAL LINE REARRANGEMENT
TOTAL NUMBER OF DEVELOPED BYTES : 64 BYTES(16 × 4)
NUMBER OF BYTES IN 1 LINE : 16BYTES
NUMBER OF DEVELOPED LINES : 4 LINES

FIG. 12A

LOCAL MEMORY

W1—

01 01	01 02	78 55	44 FF
FF FF	FF FF	FF 11	11 11
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00

FIG. 12B

W2—

01 01	01 02	78 55	44 FF
FF FF	FF FF	FF 11	11 11
62 12	77 45	89 10	55 10
10 10	10 10	10 20	20 20
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00

FIG. 12C

W3—

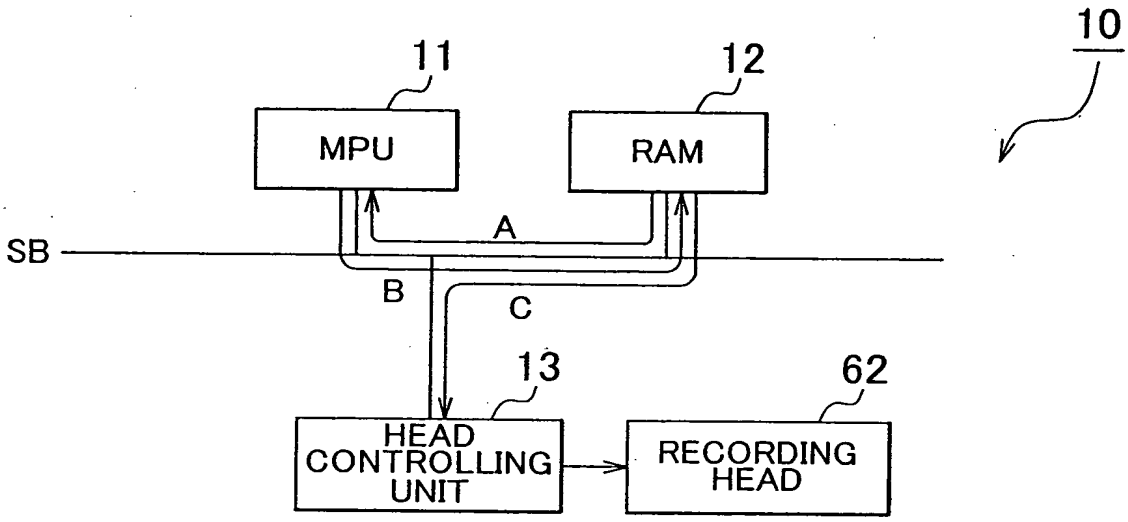
01 01	01 02	78 55	44 FF
FF FF	FF FF	FF 11	11 11
62 12	77 45	89 10	55 10
10 10	10 10	10 20	20 20
20 20	20 20	12 13	14 15
16 17	18 19	20 11	11 11
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00

FIG. 12D

W4—

01 01	01 02	78 55	44 FF
FF FF	FF FF	FF 11	11 11
62 12	77 45	89 10	55 10
10 10	10 10	10 20	20 20
20 20	20 20	12 13	14 15
16 17	18 19	20 11	11 11
11 98	B0 F2	AB AB	AB AB
AB FF	FE FC	FD FF	FF FF

FIG. 13


10
11
12
MPU
RAM
A
SB
B
C
13
62
HEAD CONTROLLING UNIT
RECORDING HEAD